IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A differential data sampling circuit comprising:

a latch circuit for sampling a differential data signal in response to a first strobe signal;

a delay element, the first strobe signal being an input to the delay element; and

a strobe circuit coupled to the latch circuit, the strobe circuit capturing the output of the latch circuit based on a second strobe signal output from the delay element.

Claim 2 (original): The differential data sampling circuit according to claim 1, wherein the latch circuit produces a voltage change at output that is less than the voltage difference between a power supply voltage that supplies the latch circuit and ground.

Claim 3 (original): The differential data sampling circuit according to claim 1,

wherein the latch circuit is an analog latch circuit that latches the differential data signal in response to the first strobe signal so as to produce a latched voltage, and

the strobe circuit samples and holds the latched voltage in order to determine a logic level of the differential data signal.

Claims 4-5 (Cancelled)

Claim 6 (currently amended): The differential data sampling circuit according to claim 1, wherein the output of the latch circuit comprises a set of differential output nodes and wherein the latch circuit includes load elements provided between a power supply input and the set of differential output nodes, ~~and~~ each of the load elements including ~~includes~~ a ~~diode-connected~~ transistor.

Claim 7 (currently amended): The differential data sampling circuit according to claim 1, wherein the latch circuit includes:

an input;

an input branch and a latch branch connected in parallel between the input and an output; and

a bias current control transistor coupled in series between the output and ~~with~~ both the input branch and the latch branch.

Claim 8 (currently amended): The differential data sampling circuit according to claim 7, wherein the input branch of the latch circuit includes:

a pair of differential input transistors electrically coupled to the input; and

a single strobe transistor coupled in series between ~~with~~ the pair of differential input transistors and the bias current control transistor.

Claim 9 (currently amended): The differential data sampling circuit according to claim 1, wherein the bias current control transistor ~~latch circuit~~ receives only one bias voltage for controlling an amount of current passing through the latch circuit.

Claim 10 (original): The differential data sampling circuit according to claim 1, further comprising a high speed differential buffer having an output coupled to the input of the latch circuit, the high speed differential buffer receiving a differential input signal.

Claim 11 (original): The differential data sampling circuit according to claim 10, wherein the differential input signal received by the high speed differential buffer is composed of a single input data signal and a reference voltage.

Claim 12 (currently amended): A digital data receiver including at least one differential data sampling circuit, said differential data sampling circuit comprising:

a latch circuit for sampling a differential data signal in response to a first strobe signal;

a delay element, the first strobe signal being an input to the delay element; and

a strobe circuit coupled to the latch circuit, the strobe circuit capturing the output of the latch circuit based on a second strobe signal output from the delay element.

Claim 13 (original): The digital data receiver according to claim 12, wherein the latch circuit produces a voltage change at output that is less than the voltage difference between a power supply voltage that supplies the latch circuit and ground.

Claim 14 (original): The digital data receiver according to claim 12,

wherein the latch circuit is an analog latch circuit that latches the differential data signal in response to the first strobe signal so as to produce a latched voltage, and

the strobe circuit samples and holds the latched voltage in order to determine a logic level of the differential data signal.

Claim 15 (Cancelled)

Claim 16 (currently amended): The digital data receiver according to claim 12, wherein the latch circuit includes:

an input that accepts the differential data signal;

an input branch and a latch branch connected in parallel between the input and an output; and

a bias current control transistor coupled in series between the output and ~~with~~ both the input branch and the latch branch.

Claim 17 (currently amended): The digital data receiver according to claim 16, wherein the input branch of the latch circuit includes:

a pair of differential input transistors electrically coupled to the input; and

a single strobe transistor coupled in series between ~~with~~ the pair of differential input transistors and the bias current control transistor.

Claim 18 (currently amended): The digital data receiver according to claim 12, wherein the bias current control transistor ~~latch circuit~~ receives only one bias voltage for controlling an amount of current passing through the latch circuit.

Claim 19 (original): The digital data receiver according to claim 12, wherein the differential data sampling circuit further includes a high speed differential buffer having an output coupled to the input of the latch circuit, the high speed differential buffer receiving a differential input signal.

Claim 20 (original): The digital data receiver according to claim 19, wherein the differential input signal received by the high speed differential buffer is composed of a single input data signal and a reference voltage.